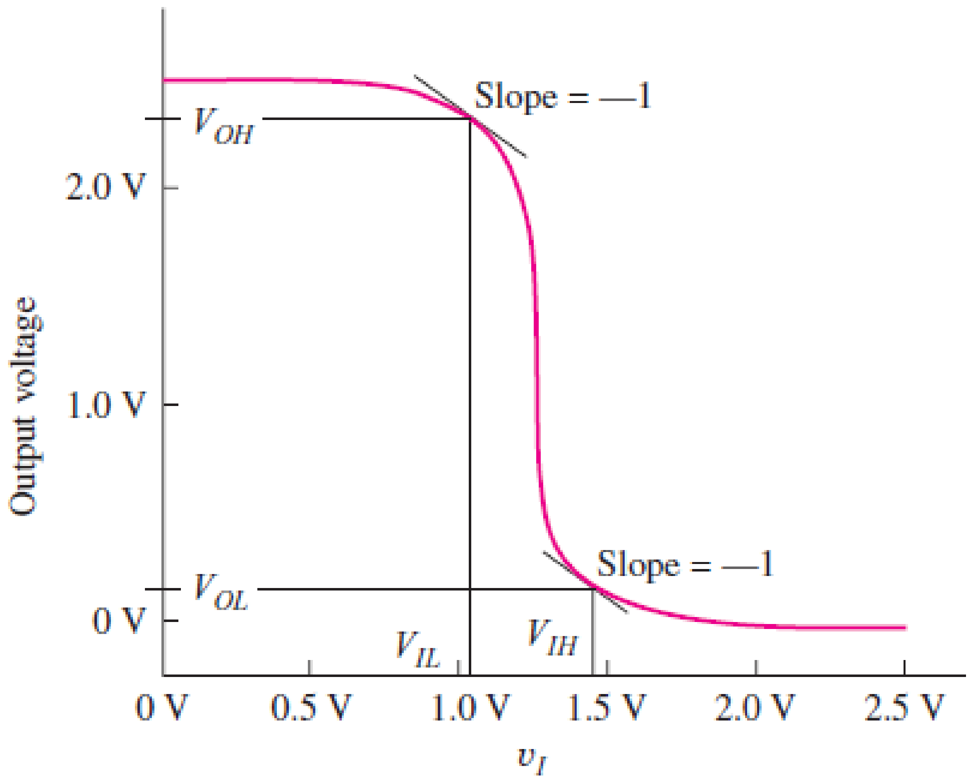
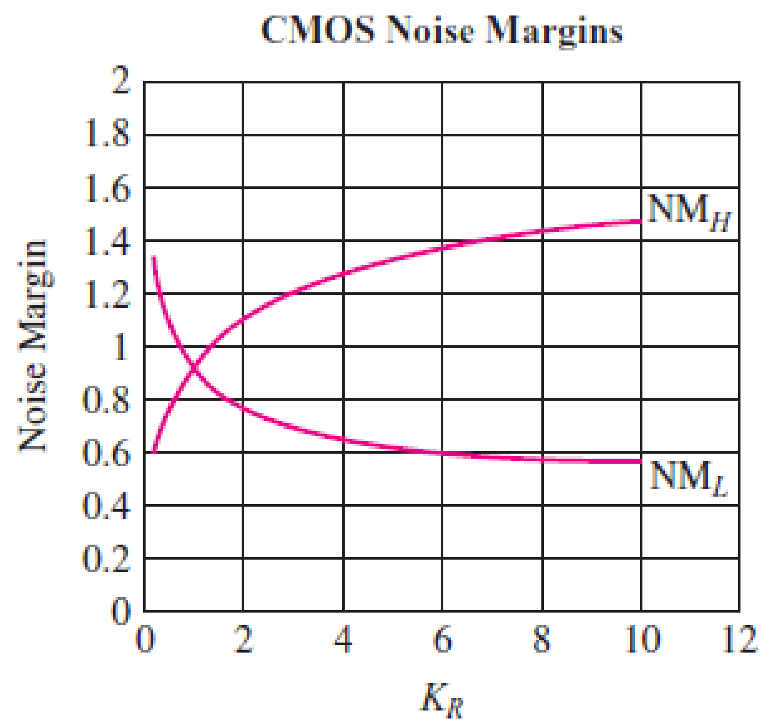
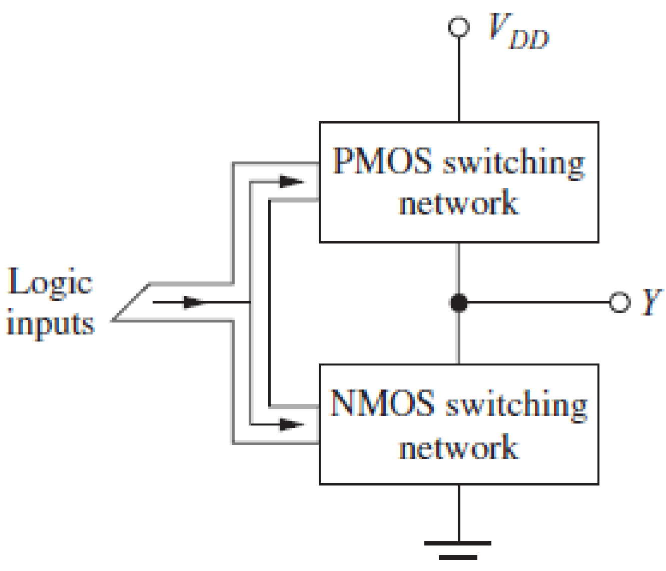
Noise Margins for the CMOS Inverter

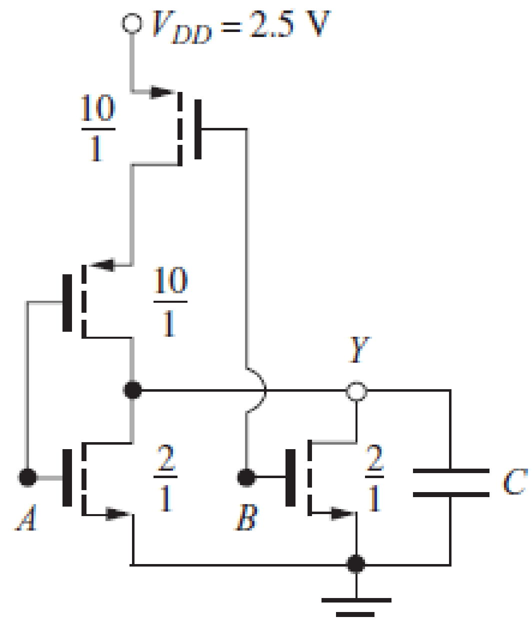


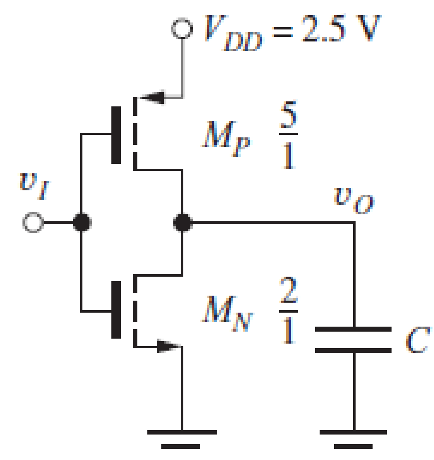


- Noise margin related to K_R
- When $K_R = 1$, $NM_H = NM_L = 0.93$ V (better than NMOS)

CMOS NOR Gate







CMOS NOR gate

Reference Inverter

- In general, a parallel path in the NMOS network corresponds to a series path in the PMOS network.
- CMOS NOR Gate: parallel NMOS, series PMOS.

CMOS NOR Gate Sizing

- When sizing the transistors, the R_{on} on the PMOS branch of the NOR gate must be the same as the reference inverter (to keep the delay times equal under the worst-case conditions)

- For a two-input NOR gate, the $(W/L)_p$ must be made twice as large

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Three-Input NOR Gate Layout

- It is possible to extend this same design technique to create multiple input NOR gates

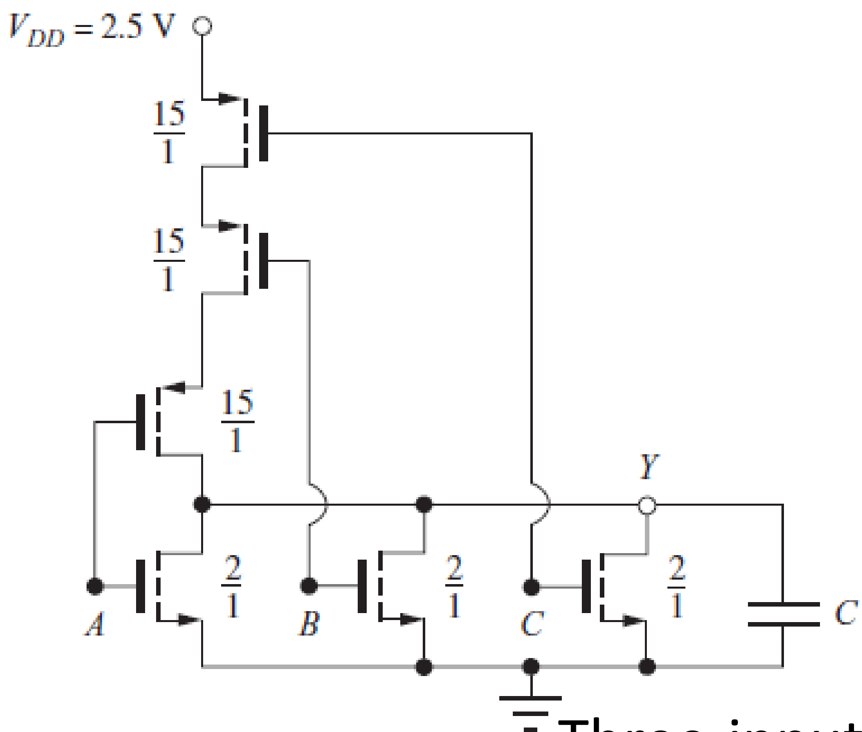

TABLE 7.4
Three-Input NOR Gate Truth Table

A	B	C	$Y = \overline{A + B + C}$
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Three-input CMOS NOR gate: $Y = \overline{A + B + C}$

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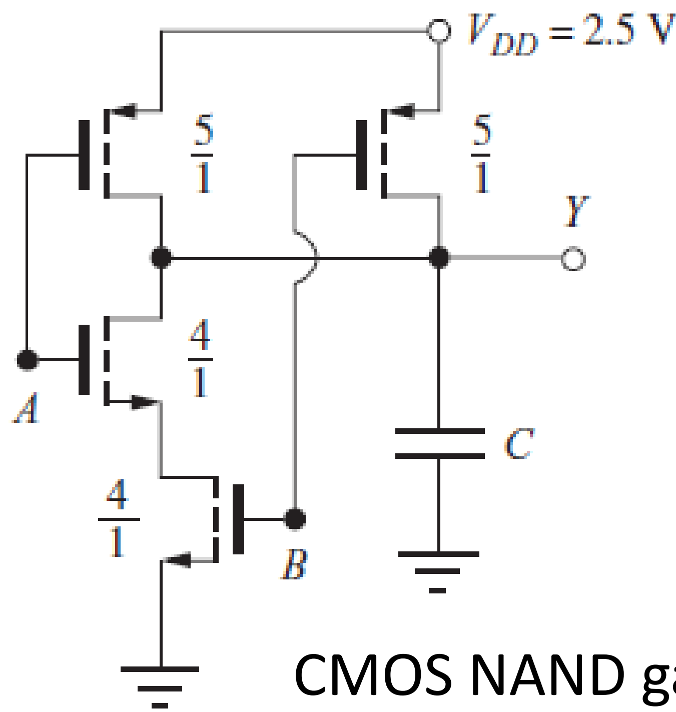
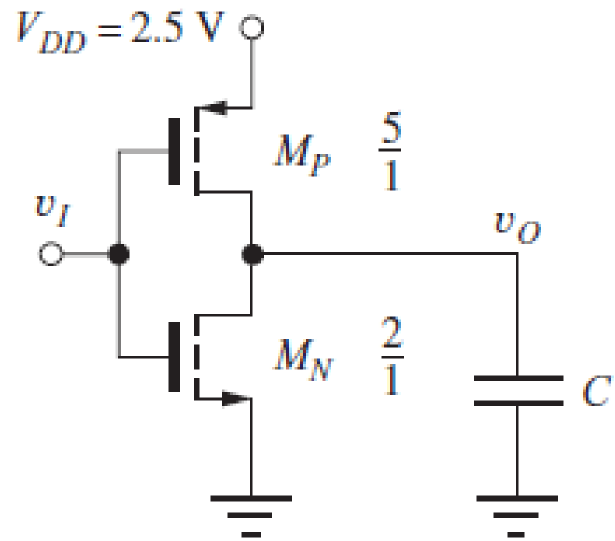
CMOS NAND Gates



CMOS NAND gate



Reference Inverter

- In general, a series path in the NMOS network corresponds to a parallel path in the PMOS network.
- CMOS NAND Gate: series NMOS, parallel PMOS.

CMOS NAND Gates Sizing

- The same rules apply for sizing the NAND gate as the did for the NOR gate, except for now the NMOS transistors are in series

- The $(W/L)_N$ will be twice the size of the reference inverter's NMOS

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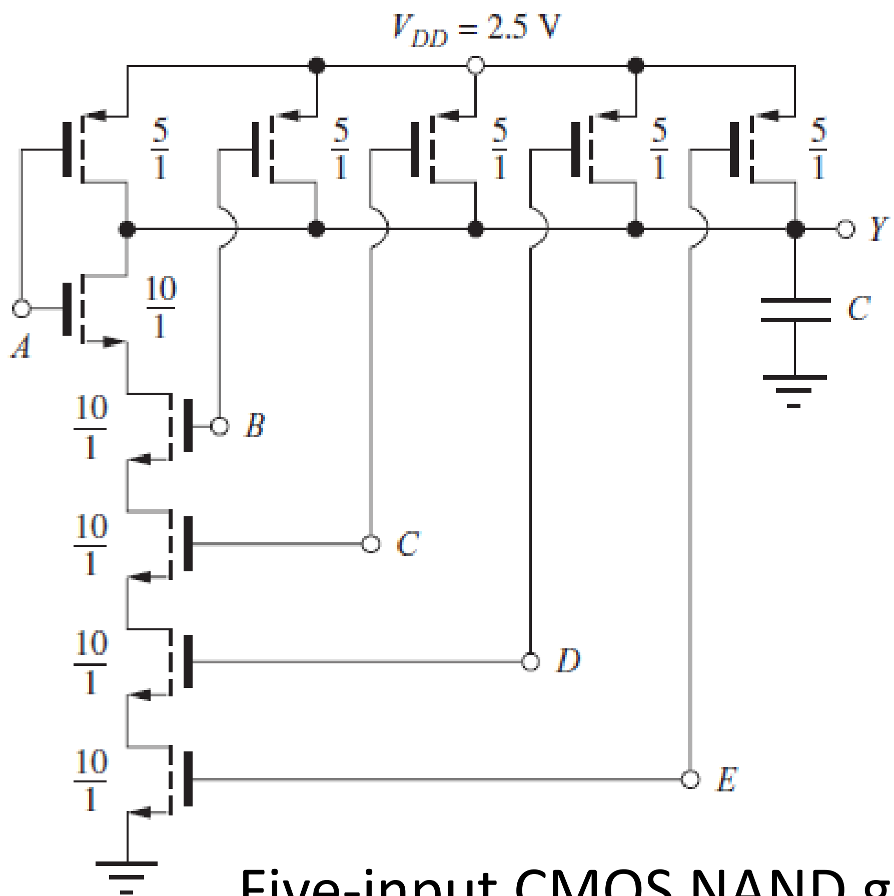
Multi-Input CMOS NAND Gates



Five-input CMOS NAND gate: $Y = \overline{ABCDE}$

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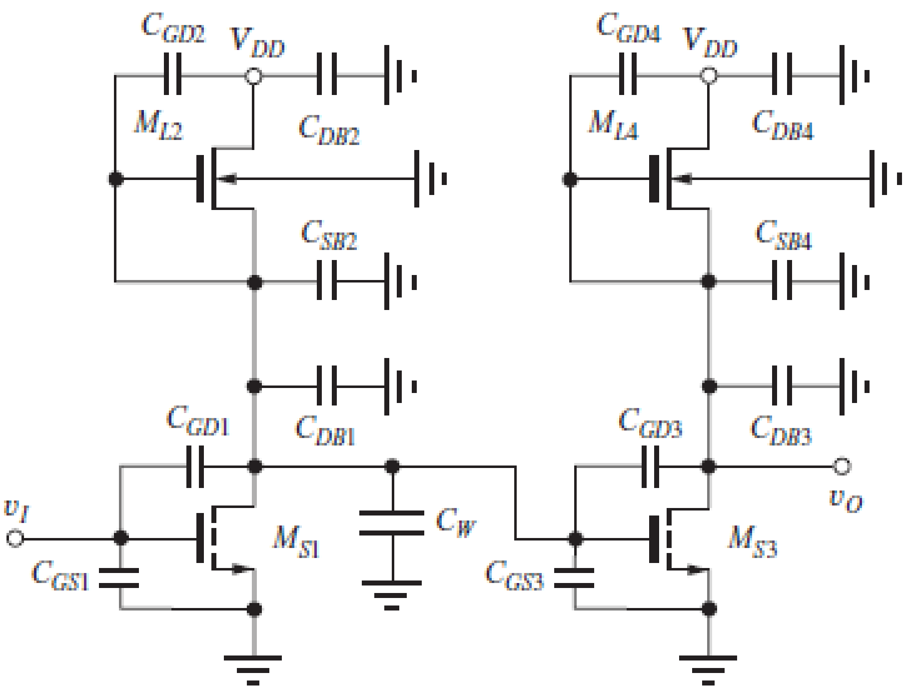
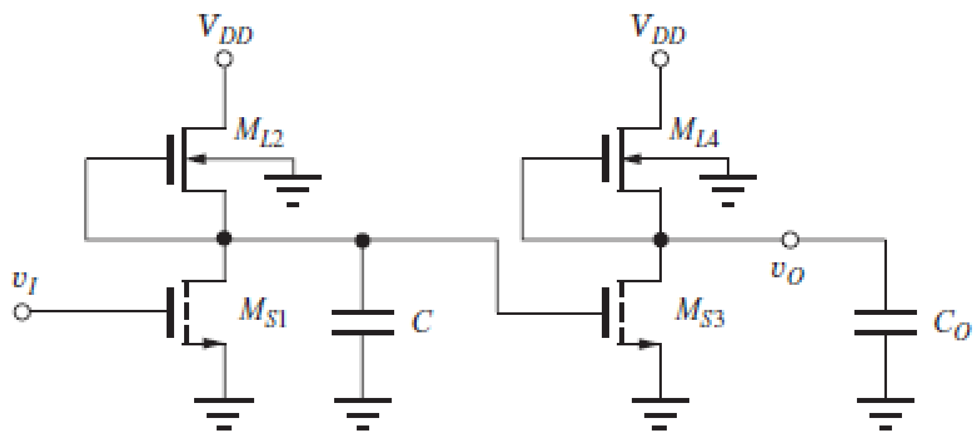
Capacitances in Logic Circuits



Various capacitances associated with transistors



The capacitances on a given node can be lumped into a fixed effective nodal capacitance *C*

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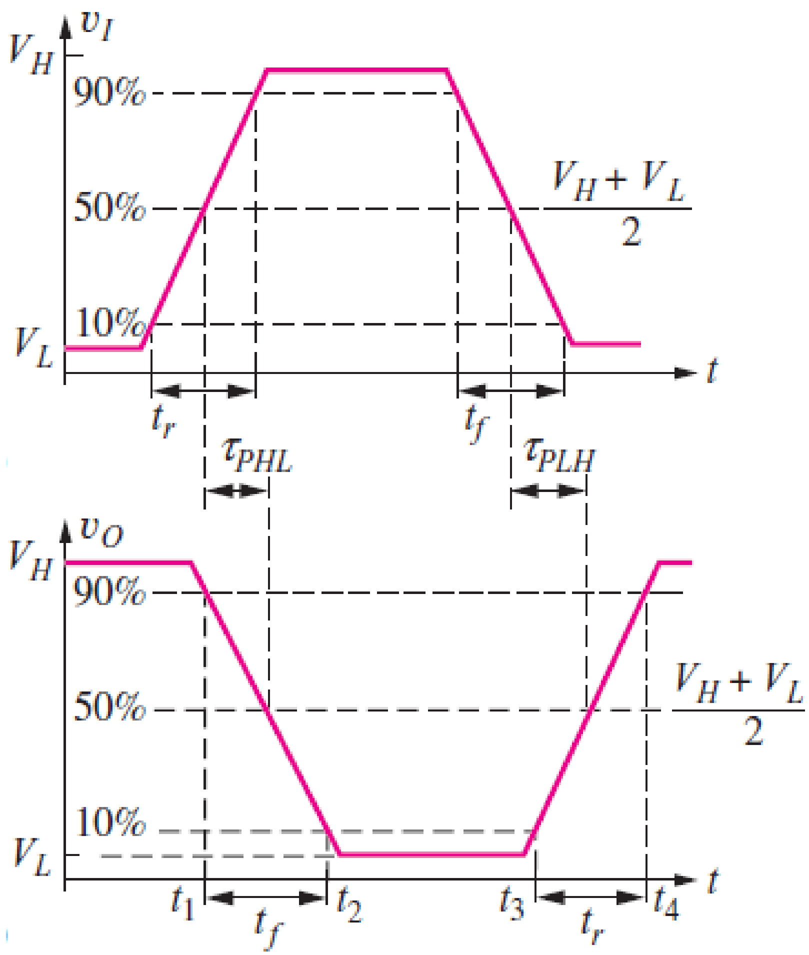
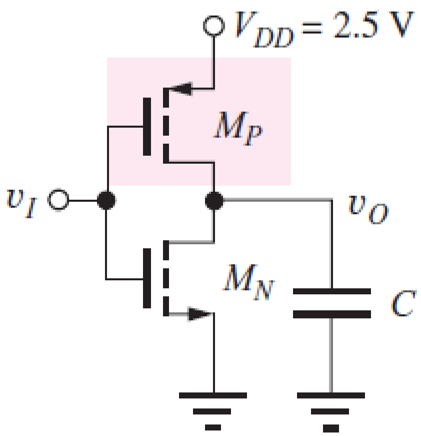
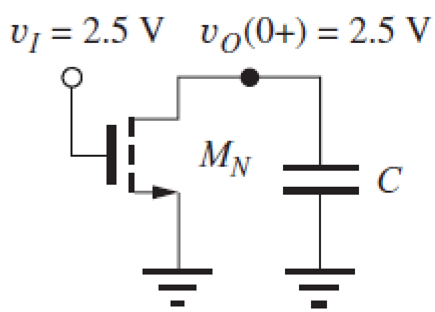
Logic Gate Dynamic Responses

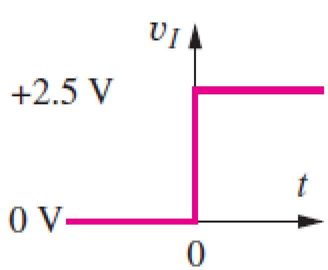


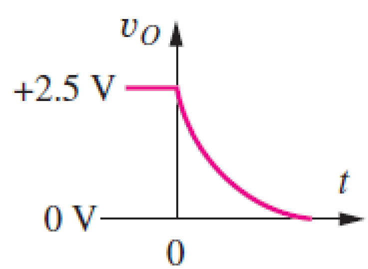
- **Rise time (t_r)**: time required from 10% point to 90% point
- **Fall time (t_f)**: time required from 90% point to 10% point
- **Propagation delay (τ_P)**: difference in time between the input and output signals reaching the 50% points
  - for output high-to-low: τ_{PHL}
  - for output low-to-high: τ_{PLH}
  - average propagation delay $\tau_P = (\tau_{PLH} + \tau_{PHL})/2$

Dynamic Response of CMOS Inverter







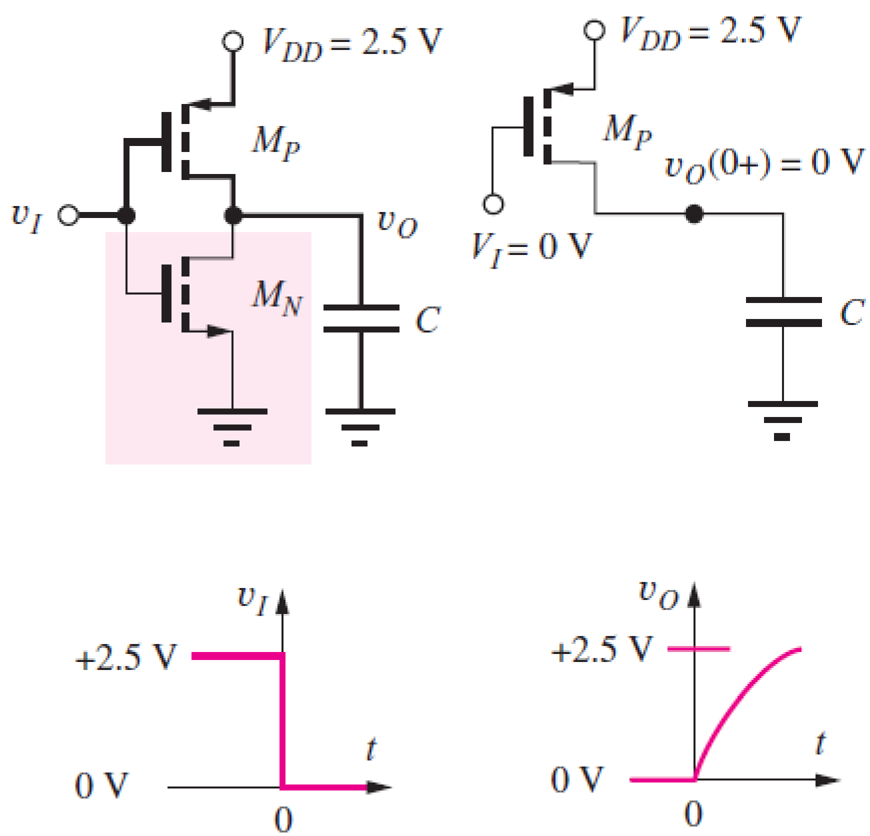


- Assume abrupt V_I change from V_L to V_H
- V_O changes from V_H to V_L by discharging C via M_N
- Same as the resistive load

$$\tau_{PHL} = 1.2 R_{\text{onn}} C$$

$$R_{\text{onn}} = \frac{1}{K_n(V_H - V_{TN})}$$

Dynamic Response of CMOS Inverter



- Assume abrupt V_I change from V_H to V_L
- V_O changes from V_L to V_H by charging C via M_P
- Similarly we get

$$\tau_{PLH} = 1.2 R_{\mathrm{onp}} C$$

$$R_{\mathrm{onp}} = \frac{1}{K_p(V_H + V_{TP})}$$

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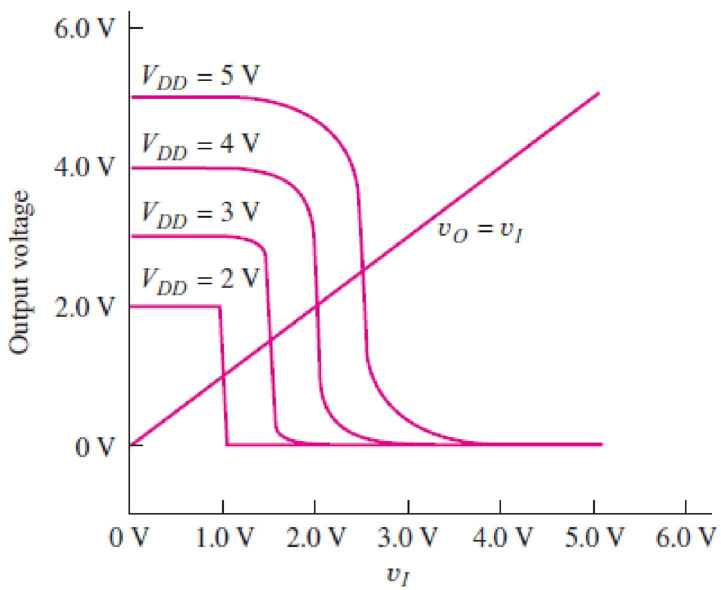
CMOS Inverter with Symmetrical Delay

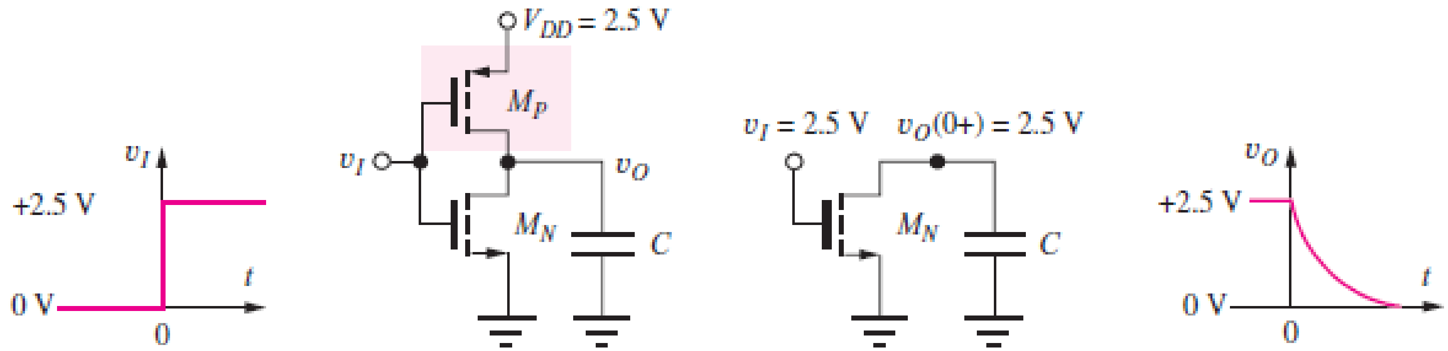
- CMS inverter with symmetrical delay has $\tau_{PLH} = \tau_{PHL} \Rightarrow R_{\text{onn}} = R_{\text{onp}} \Rightarrow K_n = K_p$
- This is exactly the "symmetrical" inverter



$$\mu_n = 2.5\mu_p \Rightarrow \left(\frac{W}{L}\right)_p = 2.5\left(\frac{W}{L}\right)_n$$

$$\tau_P = \frac{\tau_{PLH} + \tau_{PLH}}{2} = 1.2 R_{\text{onn}} C$$

CMOS Switching Speed



- Can estimate switching time for capacitive load very simply:

$$\Delta t = \frac{C_{\text{total}}\Delta v}{i_{\text{avg}}} = \frac{\Delta Q}{i_{\text{avg}}}$$

- For τ_{PHL}, v_I=V_{DD}, PMOS OFF, NMOS ON.
- NMOS saturated for $v_O > V_{DD}$-V_{TN}, linear for $v_O < V_{DD}$-V_{TN}
- Just the opposite for LH transition.

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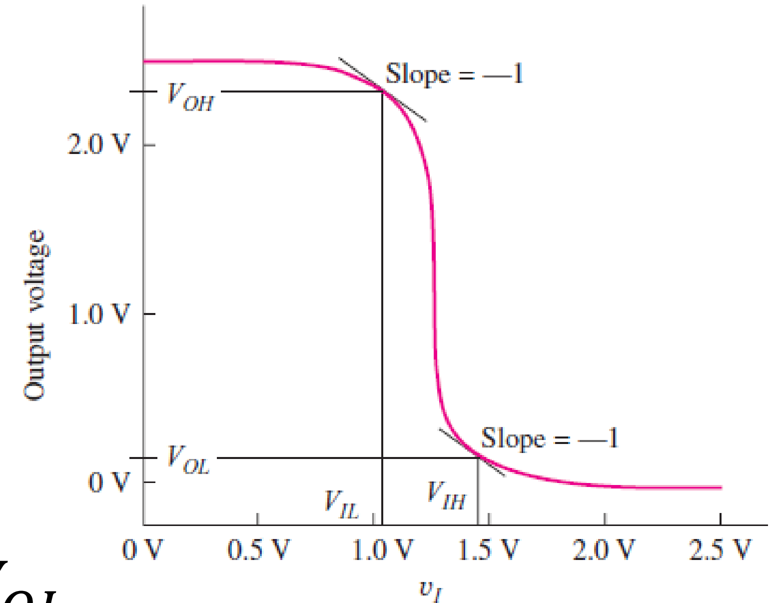
Symmetrical CMOS Inverter

- Symmetrical CMOS inverter:
  - $K_n = K_p, V_{Tn} = -V_{Tp} = V_T$
  - $\tau_{PLH} = \tau_{PHL}, R_{\text{onn}} = R_{\text{onp}}$
- If $V_T < V_{DD}/2$
  - $V_{OL} = \frac{V_{DD}}{8} - \frac{V_T}{4}, V_{OH} = V_{DD} - V_{OL}$
  - $V_{IL} = \frac{3V_{DD}}{8} + \frac{V_T}{4}, V_{IH} = V_{DD} - V_{IL}$
  - $NM_L = NM_H = \frac{V_{DD}}{4} + \frac{V_T}{2}$



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CMOS Performance Scaling

- $\tau_P = \frac{\tau_{PHL}+\tau_{PLH}}{2}$
  - $\tau_P \propto C$
  - $\tau_P \propto R_{\text{on}} \propto \left(\frac{W}{L}\right)^{-1}$
- Delay is proportional to total load capacitance *C*, and inversely proportional to W/L.
- Larger size (larger W/L) => shorter delay

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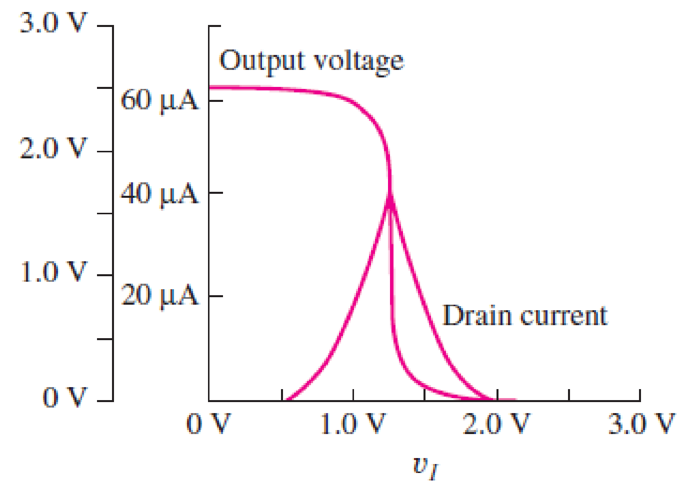
Power Dissipation

- Switching: CV_{DD}^2 per cycle
- Transition conduction: when $V_{TN} < v_{in} < V_{DD}+V_{TP}$, both transistors are on.
  - Depends on amount of time with $v_{in} \sim V_{DD}/2$ (t_r, t_f).
  - Can be 20-30% of CV_{DD}^2



- Subthreshold conduction: small currents even when devices are "off."

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